EVMINI 1.2

Evaluation Kit

Revision 0.9

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This document is preliminary and is
subject to change without notice

STMicroelectronics

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1. Motherboard Functionnal Specifications

The EVMINI 1.2 system board is a high-performance personal computer system board based on a STPC Client microprocessor (or STPC Consumer) running with an external clock of 14.31818 MHz.

This system board integrates an IDE controller, two serial ports, one parallel port as well as keyboard and PS2 type mouse interface. This is controlled by the PC87306-IBE/VUL Super I/O Circuit.

1.1 EVMINI at a glance

STPC:

- Supports socketted DX-66, DX-75, DX2-100, or DX2-120 STPC Client.

Cache memory:

- Integrated L1 write back cache.
- No L2 cache subsystem can be installed.

Main memory:

- Supports four 64-bit memory banks using four single-sided or double-sided 72-pin SIMM modules.

Slots:

- 3 x 32-bit PCI Bus slots.
- 3 x 16-bit ISA slots

Interfaces:

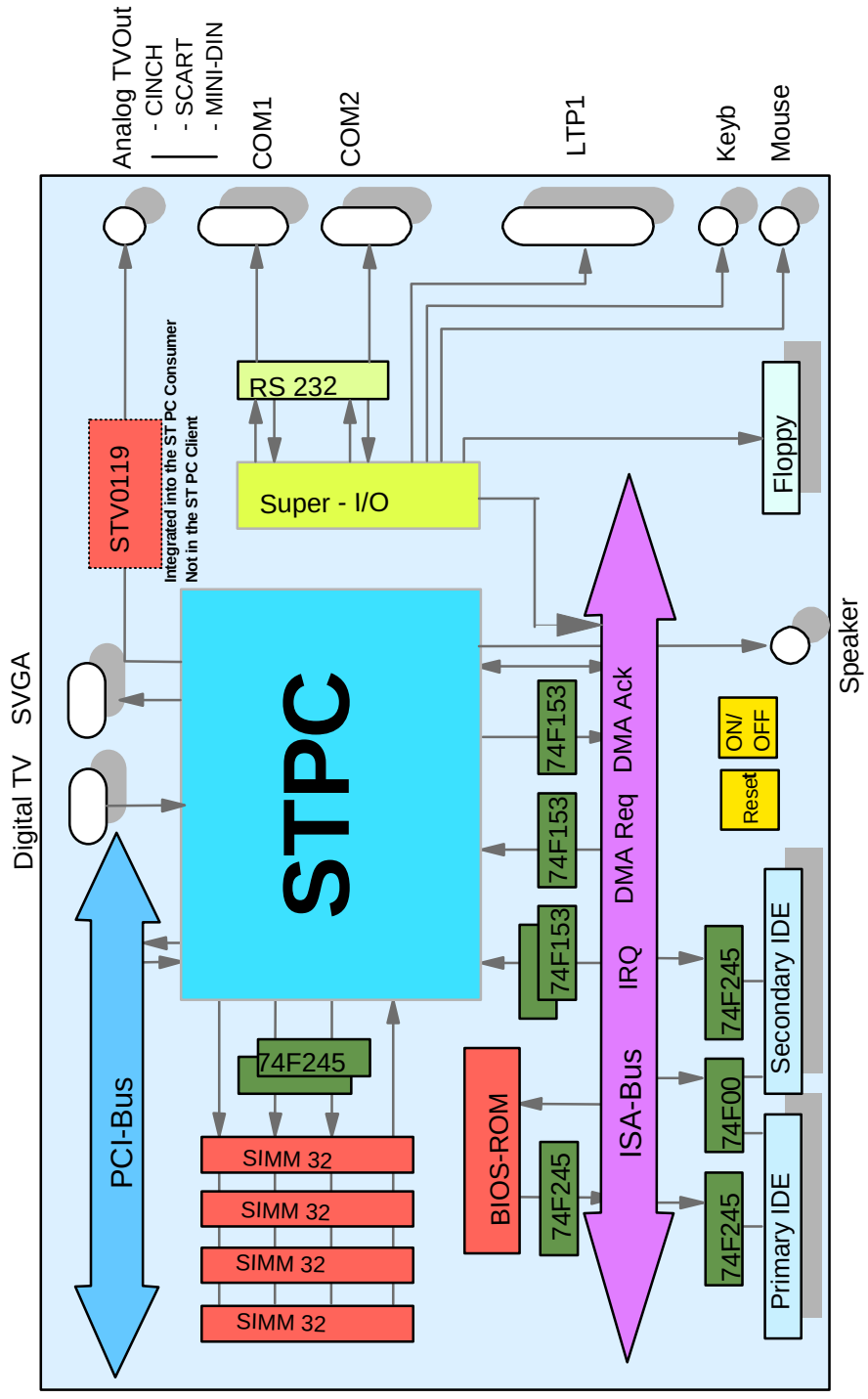
- AT and ATX power supply.
- Keyboard, Mouse, one parallel, two serials.
- Floppy, IDE master, IDE slave.
- SVGA monitor.
- CVBS, Y-C, RGB video outputs, Standard Video Input Port.
- Speaker, Reset button, ATX Power Switch button.

Dimensions:17.5 cm x 30.5 cm x 6 layers PCB.

Mounting:

10 mounting holes in ATX format

Table 1. : Block Diagram



1.2 Unified Memory Architecture

The STPC chips are built around Unified Memory Architecture. That is the same 64 bit wide array of the mother board chip set that are merged with those of advanced accelerating graphics controller by sharing. This approach reduces cost and increases performance. The major advantage of using main memory for the graphic bloc of frame buffer is lower cost (the memory is a low cost commodity DRAM) and the ability to allocate whatever memory you need to graphics without wasting memory. In using 8bit color an 800x600 display requires 470KB of memory and a 1024x768 display requires 768KB of memory but the limitations in available DRAM sizes virtually force the manufacturers to use 1MB frame buffers with consequent waste of memory. From the point of view of performance, the 64-bit wide memory array provides the system with a 200MB/s bandwidth compared with the 100MB/s bandwidth of a typical 32-bit wide memory. The 64-bit wide memory is very helpful on the graphic side because higher bandwidth allows larger screens and greater color depth.

1.3 STPC CPU Core

The CPU Core is an ST486 device that run up to 75MHz in DX mode, or 120MHz in DX2 mode. The 8 kByte cache can be configured to run in traditional write-through mode or in the higher performance write-back mode. The Floating Point Unit (FPU) is included in the core allowing parallel processing of floating point instructions.
System Management Mode (SMM) provides an additional interrupt and address space that can be used for system power management or software transparent emulation of IO peripherals. While running in isolated SMM address space, the SMM interrupt routine can execute without interfering with the operating system or application programs.
Further power management facilities include a suspend mode that can be initiated from either hardware or software resulting in a power consumption figure < 0.5 mA. Because of the static nature of the core, no internal data is lost.

1.4 STPC Integrated Chipset Functions

- Two 8237/AT compatible 7-channel DMA controller
- Two 8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Coprocessor Error support logic.
- Power Management and clock/reset unit
- Programmable system activity detector
- Support for ST SMI & SMM
- Supports SUSP#
- Slow system clock down to 8MHz
- Slow Host clock down to 8Hz
- Slow graphic clock down to 8Hz
- Supports I/O trap & restart
- Supports APM

- Independent peripheral time-out timer to monitor video, disks, serial and parallel ports.
- Supports RTC,interrupts and DMAs wake up
- 128K SMM_RAM address space from 0xA0000 to 0xB0000
- Supports General purpose I/O's

1.5 Memory Interface

The STPC Client implements a 64-bit single memory subsystem for both the system as well as the frame buffer memory. In other words, the size of the DRAM available to the system is reduced by the size of the DRAM allocated to the frame buffer.
Here below are listed the major features of the memory controller:

- Integrated system memory and graphic memory.
- Supports up to 128 MByte system memory in 4 banks.
- Supports 256KB up to 32MB single-sided and double-sided DRAM SIMMs.
- Four Double-word write buffers for CPU to DRAM and PCI to DRAM cycles.
- Four Double-wrod read prefetch buffers for PCI masters.
- Supports Fast Page Mode EDO DRAM.
- Programmable timing for DRAM parameters including CAS pulse width, CAS pre-charge time, and RAS to CAS delay
- Hidden refresh.
- Supports memory hole from 1MByte up to 8Mbyte for PCI/ISA devices.
- Shadow memory support for C, D, E, and F blocks.
- Supports memory remap for unused D and E blocks to top of system memory.

The DRAM banks must be equipped with 72-pin SIMMs. Parity is ignored. Fast Page Mode and EDO are supported.

The rules for supported SIMM combinations are:

- If both banks are populated, they are populated with the same amount of memory.
- The lowest numbered bank is filled first.

Although system DRAM data bus is 64-bit wide, 32-bit DRAM bank is also supported by not populating the upper Dword SIMM module for that particular bank but there is a performance degradation due to loss of bandwidth. Graphics and Video features are not functionnals in that case.

1.6 PCI bus interface

- 3 PCI slots fully compliant with PCI version 2.1 specifications.
- Integrated PCI arbitration interface (32 bit wide, 5V).
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.

- 1/3x and 1/2x STPC clock PCI clock.
- The STPC occupies Device number 0 slot on the PCI bus.

1.7 ISA bus interface

- 3 full ISA extension connector.
- The STPC generates the ISA clock from External 14.318Mhz oscillator clock.
- Supports programmable extra wait state for ISA cycles.
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.

1.8 Super I/O

On board Super I/O (National PC87306 IBE/VUL) provides:

- a PC-AT keyboard interface on mini DIN 6 connector.
- a PS/2 mouse interface on mini DIN 6 connector.
- a floppy disk interface on 34-pin connector.
- COM1 & COM2 on 9-pin connectors.
- a parallel port.
- a fully compatible RTC including Clock registers and Bytes of non -Volatile RAM.

1.9 EIDE

An EIDE (Extended Intelligent Drive Electronics) is provided by the STPC to connect intelligent drives that integrate the controller (HD, CD-ROM etc.). This port supports LBA (Logic Block Addressing) that allows the use of HD larger than 528MBytes. To enhance the performance, this port supports DMA F type of transfers.

1.10 Graphics

Graphics functions are performed by the STPC. The CRTC controller supports up to 1280X1024 display resolutions at 75HZ refresh rates as defined by *VESA Monitor Timing Standard*. The horizontal timing control fields are all VGA compatible. The vertical timings are extended by 1-bit to accommodate above display resolution. The address registers are extended to allow locating the frame buffer in anywhere within the first 4MB of physical main memory. Here below are listed the major features of the graphic controller

- High performance 64-bit windows accelerator.
- Complete backward compatibility to the IBM VGA and SVGA standards.
- Hardware acceleration for Text (generalized bit map expansion), bitblts and fills.

- 8, 16, 24 and 32-bit pixels.
- Up to 4MB long linear frame buffer.
- The output is an analog RGB format, Interlacing is NOT supported

1.11 Video features.

A TV Output is provided by the STPC. The NTSC/PAL encoding (conform to the NTSC/PAL timing specifications) is done by an STV0118 or STV0119 encoder when using a STPC Client, and by the integrated STV0119 when using a STPC Consumer. Three analog output are simultaneously delivered (RGB, Composite and Luma/Croma SVHS compatible). In addition to this, a Video Input Port is present on chip, which takes a video stream and store the uncompressed data on a local video buffer before displaying the full motion sequences through the TV encoder. The STPC provides the capability to superimpose On Screen Display (OSD).

2. Hardware Installation

When you install the system board, you must configure components, set jumpers, and attach connectors.

2.1 Jumpers

Jumpers

Jumpers on the system board provide information to your system about installed options and system settings. You need to configure jumpers when you install the CPU or clear CMOS memory.

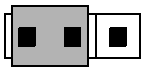
Setting Jumpers

Configure system board option by setting jumper switches.

Note: When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't loose it.

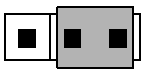
Symbols:

For 3-pin jumpers, the following symbols are used:



1 2 3

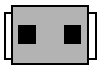
- Close pins 1 and 2 with a jumper cap.



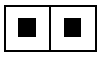
1 2 3

- Close pins 2 and 3 with a jumper cap

For 2-pin jumpers, the following symbols are used:



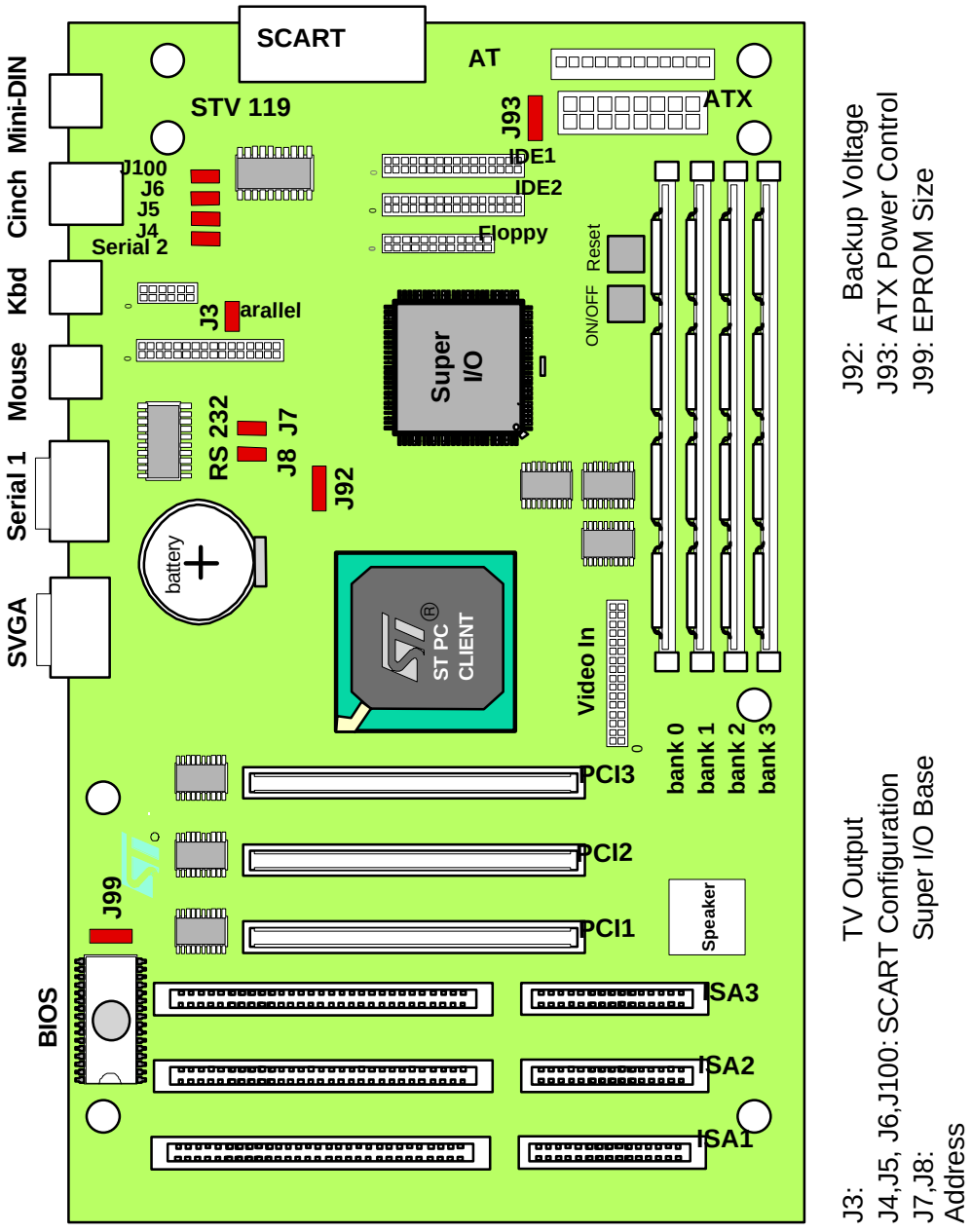
- Close the jumper by inserting the jumper cap over the two pins of the jumper.



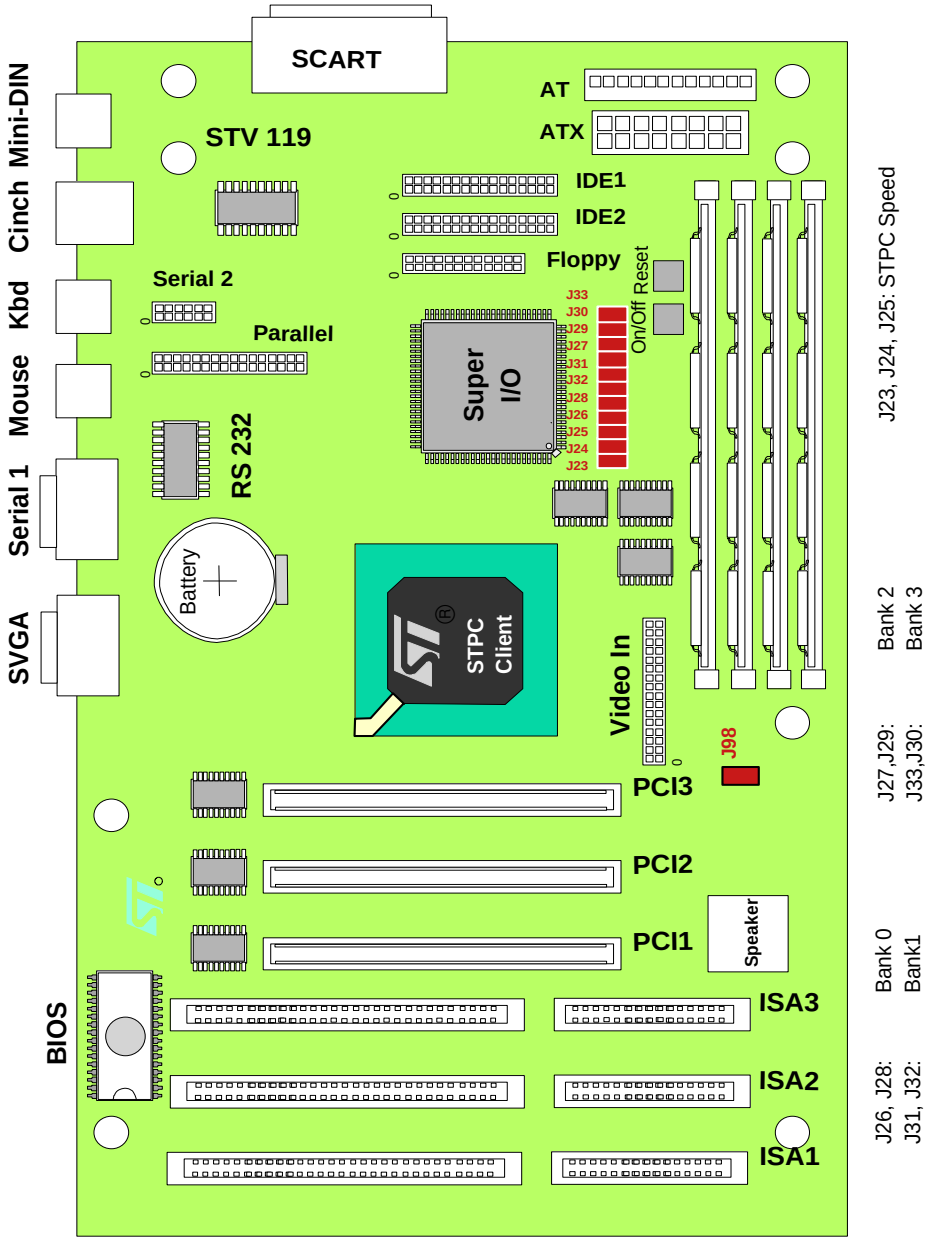
- Open the jumper by inserting the jumper cap over one or no pin(s) of the jumper.

2.2 Jumpers location

2.2.1 Configuration Jumpers

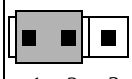
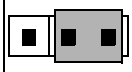
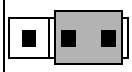
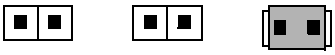


2.2.2 Strap Options



2.2.3 Default Jumper setting.

TABLE 2. Default jumper setting

Jumper	Purpose	Setting
J3	TV Output	
J4,J5,J6,J100	SCART Configuration	J4 J5 J6 J100 
J7,J8	Super I/O Base Address	J7 J8 
J92	Backup Voltage	 1 2 3
J93	ATX Power Control	 1 2 3
J99	EPROM Size	 1 2 3
J23,J24,J25	STPC Speed	J23 J24 J25 
J98	PCI Clock Speed	
J26,J28	DRAM Bank 0 Type and Speed	J26 J28 
J32,J31	DRAM Bank 1 Type and Speed	J32 J31 
J27,J29	DRAM Bank 2 Type and Speed	J27 J29 
J30,J33	DRAM Bank 3 Type and Speed	J30 J33 

2.3 Installation

For mainboard installation, it is important that the jumper settings are set correctly. Improper jumper settings will cause system instability or system hang-ups. Please refer to the installation procedures below.

2.3.1 Step 1: Verify STPC Client is correctly inserted on the socket.

STPC Client should be plugged accordingly to picture of the board on cover page. Pin A1 on device is bottom left on this image: (It corresponds to the arraw designed on the socket0

2.3.2 Step 2: Installing the SIMM Modules into the proper SIMM sockets.

This mainboard supports only 4 sockets for memory modules, U8, U9, U10, U11. Bank 0 and Bank 1 (U8, U9) must be populated to have SVGA interface working. The table below list the possible configurations for U8-U9 and for U10-U11. Using double-sided SIMM modules allows to populate the 4 banks.

TABLE 3. SIMM Module configurations

U8, U9
512Kx32
1Mx32
2Mx32
4Mx32
8Mx32
16Mx32

U10-U11
512Kx32
1Mx32
2Mx32
4Mx32
8Mx32
16Mx32

2.3.3 Step 3: Clear CMOS memory.

- Switch off the board
  - SW2 push button for ATX power supply
  -Interruptor on AT power supply
- Place J92 in 2-3 position for 2 seconds and then replace it in 1-2 position (default).

2.3.4 Step 4: Use default jumper setting to run BIOS setup.

Power, keyboard, mouse and screen must be correctly connected.

- Switch on the board.
- Select F2 (BIOS Default Values) when resquested on screen.
- Quit saving Configuration.
- Reset the board with SW1 push button.
- Press 'DEL' to launch BIOS SETUP again.
- Goto Setup menu 'Chipset Setup//DRAM Bank 0'.
- Configure DRAM Type and Speed accordingly to plugged memory modules.
- Same for banks 1, 2, and 3.
- Goto Setup menu 'Chipset Setup//DRAM Type/Timing'.
- Select 'User Setup'.
- Quit saving Configuration.

2.3.5 Step 5: Setting the STPC Speed Jumper (J23,J24,J25)

Set jumpers J23, J24 and J25 according to the speed of the STPC that is installed. This is validated on reset or Power up. This speed correspond to HCLK clock. For DX2 devices, CPU core runs at twice this speed.

!Warning: *Improper speed setting might cause serious damage to DX2 STPCs.*

TABLE 4. J23,J24,J25 settings

Setting	J23	J24	J25
25MHz			
50MHz			
60MHz			
66MHz			
75MHz			

2.3.6 Step 6: Setting the DRAM

Set Jumpers J26, J32, J27 and J30 according to the EDO and FPM MOde DRAM for Bank 0, 1, 2 and 3 respectively.

Set Jumpers J28, J31, J29, and J33 accordind to the speed of DRAM for Bank 0, 1, 2, and 3 respectively.

Table 5. Bank 0 setting

Setting	J26
FPM	
EDO	

Setting	J28
60ns	
70ns	

Table 6. Bank 1 setting

Setting	J 32
FPM	
EDO	

Setting	J 31
60 ns	
70 ns	

Table 7. Bank 2 setting

Setting	J 27
FPM	
EDO	

Setting	J 29
60ns	
70ns	

Table 8. Bank 3 setting

Setting	J 30
FPM	
EDO	

Setting	J 33
60ns	
70ns	

Note:You can modify the DRAM Configuration by changing the BIOS setting (The BIOS setting has priority over the jumper setting)

2.3.7 Step 7: Setting the PCI Clock Speed (J98)

Set jumper J98 according to STPC speed setup and required PCI clock speed. This is validated on reset or Power up.

TABLE 9. J98 setting

Setting	J98
HCLK / 3	
HCLK / 2	

2.3.8 Step 8: Setting the RGB / CVBS Video Output (J3)

Set jumper J3 according to requested TV Output. SCART connector is configured to generate RGB only. CINCH connector generates CVBS only.Software Installation

TABLE 10. J3 setting

Setting	J3
CVBS	
RGB	

3. Software Installation

The EVMINI kit includes 2 floppy disks:

One for the windows drivers:

- Windows 95 Driver
  - Graphics Driver
  - Direct Draw Driver
  - MCI Driver
- Windows 3.1: Graphics Driver

The other one for EVMINI 1.2 hardware

- Schematics of the board in ORCAD and PROTEL Format
- Gerber files of the board

3.1 Windows 3.1 driver installation

- Run Windows setup.
- Choose ‘Change System Settings’ in ‘Option’ menu.
- Insert disk in Floppy drive.
- Select ‘Other display (Requires disk from OEM...’ in display list.

3.2 Windows 95 driver installation

- Open Control Panel.
- Select Display icon.
- Select Setting sheet.
- Press ‘Advanced Properties’ button.
- Press ‘Change...’ button in Adapter sheet.
- Insert disk in Floppy drive.
- Press ‘Have Disk...’ button.
- Press ‘OK’.
-
- Motherboard Hardware Specifications

4. Motherboard Hardware Specifications

4.1 Connectors

The following table contains the exhaustive list of all the connectors that is implemented on the demo board.

TABLE 11. Connector List

Identification	Name	Type	Nb of Pins
PA1,PA2,PA3	ISA (8-bit)	ISA	62
PB1,PB2,PB3	ISA (16-bit extension)	ISA	36
U14	Y-C Video Output	Mini Din	4
P1	VGA	Sub D	15
P2	Mouse	Mini Din	6
P3	Keyboard	Mini Din	6
P4	Video Input	Straight Pin header	26
P5	Parallel	Straight Pin header	26
P6	CVBS Video Output	CINCH	1
P7	SCART	SCART	21
P8,P9,P10	PCI	PCI	124
P11	COM	Sub D	9
P12	COM	Straight Pin header	10
P13	IDE - Primary	Straight Pin header	40
P14	IDE - Secondary	Straight Pin header	40
P15	Floppy	Straight Pin header	34
P17	ATX Power Supply	ATX	20
P18	Key_Lock	Straight Pin header	5
P19	AT Power Supply	AT	12
J18	Turbo	Straight Pin header	2
J19	HDLed	Straight Pin header	2
J20	ATX Control	Straight Pin header	2
J21	Reset	Straight Pin header	2
J92	CMOS Reset	Straight Pin header	3

4.1.1 Connector definition

ISA Connectors

TABLE 12. ISA Connector Pin Definition (PA1/PB1, PA2/PB2, PA3/PB3)

Signal name	Pin	Pin	Signal name
GND	B1	A1	IOCHCK#
RSTDRV	B2	A2	SD7
VCC	B3	A3	SD6
IRQ9	B4	A4	SD5
-5V	B5	A5	SD4
DRQ2	B6	A6	SD3
-12V	B7	A7	SD2
0WS	B8	A8	SD1
+12V	B9	A9	SD0
GND	B10	A10	IOCHRDY
SMEMW#	B11	A11	AEN
SMEMR#	B12	A12	SA19
IOW#	B13	A13	SA18
IOR#	B14	A14	SA17
DACK3#	B15	A15	SA16
DREQ3	B16	A16	SA15
DACK1#	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH#	B19	A19	SA12
BCLK	B20	A20	SA11
IRQ7	B21	B21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DACK2#	B26	A26	SA5
TC	B27	A27	SA4
BALE	B28	A28	SA3
Vcc	B29	A29	SA2
OSC	B30	A30	SA1
GND	B31	A31	SA0
	KEY	KEY	
MEMCS16#	D1	C1	SBHE#
IOCS16#	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21

TABLE 12. ISA Connector Pin Definition (PA1/PB1, PA2/PB2, PA3/PB3)

Signal name	Pin	Pin	Signal name
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
DACK0#	D8	C8	LA17
DRQ0	D9	C9	MEMR#
DACK5#	D10	C10	MEMW#
DRQ5	D11	C11	SD8
DACK6#	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7#	D14	C14	SD11
DRQ7	D15	C15	SD12
Vcc	D16	C16	SD13
MASTER#	D17	C17	SD14
GND	D18	C18	SD15

Y-C Video Output Connector

TABLE 13. Y-C Video Output Connector Pin Definition (U14)

Signal name	Pin
GND	1
GND	2
Y (Luminance)	3
C (Chromanance)	4
GND	5

VGA Connector

TABLE 14. Standard VGA Connector Pin Definition (P1)

Signal Name	Pin
Red	1
Green	2
Blue	3
ID2	4
GND	5
GND	6
GND	7
GND	8

TABLE 14. Standard VGA Connector Pin Definition (P1)

Signal Name	Pin
VCC Fuse	9
GND	10
ID0	11
DDCDAT	12
HS	13
VS	14
DDCCLK	15

Mouse Connector

TABLE 15. Mouse Connector Pin Definition (P2)

Signal Name	Pin
MData	1
NC	2
GND	3
MVCC	4
MClk	5
NC	6

Keyboard Connector

TABLE 16. Keyboard Connector Pin Definition (P3)

Signal Name	Pin
KBData	1
NC	2
GND	3
KBVCC	4
KBClk	5
NC	6

Video Input

TABLE 17. Video Input Connector Pin Definition (P4)

Signal Name	Pin	Pin	Signal Name
GND	1	2	D[0]
GND	3	4	D[1]
GND	5	6	D[2]
	7	8	D[3]
	9	10	D[4]
	11	12	D[5]
	13	14	D[6]
	15	16	D[7]
GND	17	18	CLK
GND	19	20	HSYNC
GND	21	22	PARITY
	23	24	
	25	26	GND

Parallel Connectors

TABLE 18. Parallel Connector Pin Definition (P5)

Signal Name	Pin	Pin	Signal Name
STROBE#1	1	14	AFD#1
DP1_0	2	15	ERROR#1
DP1_1	3	16	INIT#1
DP1_2	4	17	SLCT IN#1
DP1_3	5	18	GND
DP1_4	6	19	GND
DP1_5	7	20	GND
DP1_6	8	21	GND
DP1_7	9	22	GND
ACK#1	10	23	GND
BUSY1	11	24	GND
PE1	12	25	GND
SLCT1	13	26	NC

CVBS Video Output Connector

TABLE 19. CVBS Video Output Connector Pin Definition (P6)

Signal name	Pin
VIDEO	1
GND	2

SCART Connectors

TABLE 20. SCART Connector Pin Definition (P7)

Signal Name	Pin	Pin	Signal Name
	1	2	
	3	4	GND
GND	5	6	
BLUE OUT	7	8	Pull_Up 200 / +12V
GND	9	10	
GREEN OUT	11	12	
GND	13	14	GND
RED OUT	15	16	Pull_Up 82 / +5V
GND	17	18	GND
CVBS OUT	19	20	
GND	21		

PCI Connectors

TABLE 21. PCI Connector Pin Definition (P8, P9, P10)

Signal name	Pin	Pin	Signal name
GND	A1	B1	-12V
+12V	A2	B2	NC
NC	A3	B3	GND
NC	A4	B4	NC
Vcc	A5	B5	Vcc
see next 3 tables	A6	B6	Vcc
see next 3 tables	A7	B7	*see next 3 tables*
Vcc	A8	B8	*see next 3 tables*
Reserved	A9	B9	NC
Vcc	A10	B10	Reserved
Reserved	A11	B11	NC
GND	A12	B12	GND

TABLE 21. PCI Connector Pin Definition (P8, P9, P10)

Signal name	Pin	Pin	Signal name
GND	A13	B13	GND
Reserved	A14	B14	Reserved
RESET#	A15	B15	GND
Vcc	A16	B16	PCICLK
see next 3 tables	A17	B17	GND
GND	A18	B18	*see next 3 tables*
Reserved	A19	B19	Vcc
AD30	A20	B20	AD31
3.3V	A21	B21	AD29
AD28	A22	B22	GND
AD26	A23	B23	AD27
GND	A24	B24	AD25
AD24	A25	B25	3.3V
see next 3 tables	A26	B26	CBE3#
3.3V	A27	B27	AD23
AD22	A28	B28	GND
AD20	A29	B29	AD21
GND	A30	B30	AD19
AD18	A31	B31	3.3V
AD16	A32	B32	AD17
3.3V	A33	B33	CBE2#
FRAME#	A34	B34	GND
GND	A35	B35	IRDY-
TRDY#	A36	B36	3.3V
GND	A37	B37	DEVSEL#
STOP#	A38	B38	GND
3.3V	A39	B39	PCILOCK#
SDONE	A40	B40	PERR#
SBO#	A41	B41	3.3V
GND	A42	B42	SERR#
PAR	A43	B43	3.3V
AD15	A44	B44	CBE1#
3.3V	A45	B45	AD14
AD13	A46	B46	GND
AD11	A47	B47	AD12
GND	A48	B48	AD10
AD9	A49	B49	GND
KEY	A50	B50	KEY
KEY	A51	B51	KEY

TABLE 21. PCI Connector Pin Definition (P8, P9, P10)

Signal name	Pin	Pin	Signal name
CBE0#	A52	B52	AD8
3.3V	A53	B53	AD7
AD6	A54	B54	3.3V
AD4	A55	B55	AD5
GND	A56	B56	AD3
AD2	A57	B57	GND
AD0	A58	B58	AD1
Vcc	A59	B59	Vcc
NC	A60	B60	NC
Vcc	A61	B61	Vcc
Vcc	A62	B62	Vcc

TABLE 22. PCI Connector Pin Definition (P8)

Signal name	Pin	Pin	Signal name
PCI_INT1#	A6		
PCI_INT3#	A7	B7	PCI_INT2#
		B8	PCI_INT0#
PCI_GNT1#	A17		
		B18	PCI_REQ1#
IDSELB (AD30)	A26		

TABLE 23. PCI Connector Pin Definition (P9)

Signal name	Pin	Pin	Signal name
PCI_INT0#	A6		
PCI_INT2#	A7	B7	PCI_INT1#
		B8	PCI_INT3#
PCI_GNT0#	A17		
		B18	PCI_REQ0#
IDSELA (AD31)	A26		

TABLE 24. PCI Connector Pin Definition (P10)

Signal name	Pin	Pin	Signal name
PCI_INT2#	A6		
PCI_INT0#	A7	B7	PCI_INT3#
		B8	PCI_INT1#
PCI_GNT2#	A17		
		B18	PCI_REQ2#
IDSELC (AD29)	A26		

COM (Serial Port) Connectors

TABLE 25. COM (Serial Port) Connector Pin Definition (P11, P12)

Signal Name	Pin
HDCD#	1
HRxD	2
HTxD	3
HDTR#	4
GND	5
HDSR#	6
HRTS#	7
HCTS#	8
HRI#	9

IDE Connectors

TABLE 26. IDE Connector Pin Definition (P13, P14)

Signal Name	Pin	Pin	Signal Name
RST#	1	2	GND
HD7	3	4	HD8
HD6	5	6	HD9
HD5	7	8	HD10
HD4	9	10	HD11
HD3	11	12	HD12
HD2	13	14	HD13
HD1	15	16	HD14
HD0	17	18	HD15
GND	19	20	KEY

TABLE 26. IDE Connector Pin Definition (P13, P14)

Signal Name	Pin	Pin	Signal Name
DREQ	21	22	GND
XIOW#	23	24	GND
XIOR#	25	26	GND
IOCHRDY	27	28	GND
DACK#	29	30	GND
IRQ	31	32	IOCS16#
XA1	33	34	GND
XA0	35	36	XA2
HCS#0	37	38	HCS#1
Activity	39	40	GND

Floppy Connector

TABLE 27. Floppy Connector Pin Definition (P15)

Signal Name	Pin	Pin	Signal Name
GND	1	2	DENSEL
GND	3	4	Reserved
KEY	5	6	DRATE0
NC	7	8	Index#
GND	9	10	MTR#0
GND	11	12	DDR#1
NC	13	14	DR#0
GND	15	16	MTR#2
MSEN1	17	18	DIR#
GND	19	20	STEP#
GND	21	22	WDATA#
GND	23	24	WGATE#
GND	25	26	TRK0#
MSEN0	27	28	WP#
GND	29	30	RDATA#
GND	31	32	HDSEL
GND	33	34	DSKCHG

ATX Power Supply Connectors

TABLE 28. ATX Power Supply Connector Pin Definition (P17)

Signal Name	Pin	Pin	Signal Name
+3.3V	11	1	+3.3V
-12V	12	2	+3.3V
GND	13	3	GND
ON# / OFF	14	4	+5V
GND	15	5	GND
GND	16	6	+5V
GND	17	7	GND
-5V	18	8	POWER GOOD
+5V	19	9	+5V Supply Backup
+5V	20	10	+12V

Key_Lock Connector

TABLE 29. Key_Lock Connector Pin Definition (P18)

Signal name	Pin
LED_PWR	1
Key	2
GND	3
KEY LOCK	4
GND	5

AT Power Supply Connector

TABLE 30. AT Power Supply Connector Pin Definition (P19)

Signal Name	Pin
Power Good	1
+5V	2
+12V	3
-12V	4
GND	5
GND	6
GND	7
GND	8
-5V	9
+5V	10
+5V	11
+5V	12

Turbo Connector

TABLE 31. Turbo Connector Definition (J18)

Signal name	Pin
Turbo	1
GND	2

HDLed Connector

TABLE 32. Hard Drive Led Connector Pin Definition (J19)

Signal name	Pin
Pull_Up_150	1
HD Active	2

ATX Control

TABLE 33. Reset Connector Pin Definition (J20)

Signal name	Pin
ON / OFF	1
GND	2

Reset Connector

TABLE 34. Reset Connector Pin Definition (J21)

Signal name	Pin
Reset	1
GND	2

CMOS Reset Jumper

TABLE 35. CMOS Reset Jumper Pin Definition (J92)

Signal name	Pin
Battery	1
VBAT	2
GND	3

TABLE 36. STPC Client- Power on strap use on EVMINI1.2 board

Note: Bold and italic lines refer to default settings

Function	Name				Purpose
TV Output	**J3**				**Select TV Output reference signal**
	open				CVBS Output
	close				***RGB Output***
SCART Configuration	**J4**	**J5**	**J6**	**J100**	**Set Video Output on Scart Configuration**
	close	***open***	***open***	***close***	***RGB/SVHS/CVBS signals***
Super I/O Base Address	**J7**	**J8**			**Base Address selection**
	open	open			0x398
	open	close			0x26E
	close	open			0x15C
	close	***close***			***0x2E***
Backup Voltage	**J92**				**CMOS parameters used**
	1-2				***Current CMOS RAM parameters (normal operation)***
	2-3				Force ATX power supply on
ATX power control	**J93**				**Specify ATX power mode**
	1-2				force ATX power supply on
	2-3				***Switch and software control***
	open				Force ATX power supply off
EPROM size	**J99**				**Define the size of BIOS EPROM**
	1-2				1MBytes
	2-3				***2MBytes***
STPC Speed	**J23**	**J24**	**J25**		**Specify the CPU frequency (HCLK)**
	open	open	open		75MHz
	open	***open***	***close***		***66MHz***
	open	close	open		60MHz
	open	close	close		50MHz
	close	open	open		25MHz
	close	open	close		reserved
	close	close	open		reserved
	close	close	close		reserved
PCI Clock Speed	**J98**				**Specify the PCI bus frequency**
	open				HCLK/3
	close				***HCLK/2***
DRAM Bank0 Type	**J26**				**Specify the type of memory chip for bank0**
	open				***Fast Page Mode (FPM) DRAM***
	close				Extended Data Out (EDO) DRAM

TABLE 36. STPC Client- Power on strap use on EVMINI1.2 board

Note: Bold and italic lines refer to default settings

Function	Name				Purpose
DRAM Bank0 Speed	**J28**				**Specify the speed of memory chip for Bank0**
	open				60ns
	close				***70ns***
DRAM Bank1 Type	**J32**				**Specify the type of memory chip for Bank1**
	open				***Fast Page Mode (FPM) DRAM***
	close				Extended Data Out (EDO) DRAM
DRAM Bank1 Speed	**J31**				**Specify the speed of memory chip for Bank1**
	open				60ns
	close				***70ns***
DRAM Bank2 Type	**J27**				**Specify the type of memory chip for Bank2**
	open				***Fast Page Mode (FPM) DRAM***
	close				Extended Data Out (EDO) DRAM
DRAM Bank2 Speed	**J29**				**Specify the speed of memory chip for Bank2**
	open				60ns
	close				***70ns***
DRAM Bank3 Type	**J30**				**Specify the type of memory chip for Bank3**
	open				***Fast Page Mode (FPM) DRAM***
	close				Extended Data Out (EDO) DRAM
DRAM Bank3 Speed	**J33**				**Specify the speed of memory chip for Bank3**
	open				60ns
	close				***70ns***

4.3.2 BOM when using STPC Client

EVMINI1.2 Client Revised: May 8, 1998
Revision: 1.2

Bill Of Materials May 8, 1998 3:18:11

Item	Quantity	Reference	Part
1	1	B1	3.0V COIN
2	10	C1,C144,C145,C146,C147, C148,C149,C150,C151,C152	10nF 0805
3	69	C2,C3,C4,C5,C6,C7,C8,C9, C10,C11,C12,C13,C14,C15, C16,C17,C18,C19,C20,C21, C22,C23,C24,C25,C26,C27, C28,C29,C30,C31,C32,C33, C34,C35,C36,C37,C38,C39, C40,C41,C42,C43,C44,C45, C46,C47,C48,C49,C50,C51, C52,C53,C54,C140,C153, C154,C155,C156,C157,C158, C159,C160,C161,C162,C163, C164,C165,C173,C174	.1uF 0805
4	9	C55,C56,C61,C62,C63,C64, C65,C66,C67	1uF A
5	10	C57,C58,C59,C60,C166, C167,C168,C169,C170,C171	33uF C
6	19	C68,C69,C70,C71,C72,C73, C74,C75,C76,C77,C78,C79, C80,C81,C82,C83,C84,C85, C143	22uF B
7	4	C88,C89	15pF 0805
8	4	C90,C91,C92,C93	220pF 0805
9	4	C94,C95,C96,C97	330pF 0805
10	14	C98,C99,C100,C101,C102, C103,C104,C105,C131,C132, C133,C134,C135,C136	390pF 0805
11	4	C106,C107,C108,C109	3.3nF 0805
12	11	C110,C111,C112,C113,C114, C115,C116,C117,C118,C119, C120	47pF 0805
13	2	C121,C122	680pF 0805
14	8	C123,C124,C125,C126,C127, C128,C129,C130	470pF 0805
15	3	C137,C138,C139	10uF B
16	2	C141,C142	22uF_16V D
17	1	C172	220uF B
18	1	D1	LM385BZ TO92
19	12	D2,D3,D4,D5,D6,D7,D8,D9, D10,D11,D12,D13	1N4148 SOT23
20	4	D14,D15,D16,D17	BAR43 SOT23
21	4	DL1,DL2,DL3,DL4	LED SOT23 *
22	2	FB1,FB2	FBEAD FERRITE
23	1	HP1	SPEAKER
24	24	J1,J3,J4,J5,J6,J7,J8,J18, J19,J20,J21,J23,J24,J25, J26,J27,J28,J29,J30,J31, J32,J33,J98,J100	JUMPER_2X1 HEADER_2X1
25	17	J34,J35,J36,J37,J38,J39, J40,J41,J42,J43,J44,J45, J46,J47,J48,J49,J50	STR3CMS STR3CMS

26	2	J72,J73	TESTPIN HEADER_1X1
27	3	J92,J93,J99	HEADER_3 HEADER_3X1
28	6	L1,L2,L3,L4,L5,L6	BEAD 1206
29	4	L7,L8,L9,L10	2.7uH 1206
30	1	L11	BEAD
31	1	OS1	OSCP OSCP
32	1	OS2	27MHz
33	1	P1	DBS15F DBS15F
34	2	P2,P3	MINIDIN MINIDIN
35	2	P4,P5	HEADER_13X2 HEADER_13X2
36	1	P6	CINCH_F CINCH_F
37	1	P7	PERITEL SCART
38	3	P8,P9,P10	PCI32 PCI32
39	1	P11	CONNECTOR_DB9 DB9MC
40	1	P12	HEADER_5X2 HEADER_5X2
41	2	P13,P14	HEADER_20X2 HEADER_20X2
42	1	P15	HEADER_17X2 HEADER_17X2
43	1	P17	ATX ATX
44	1	P18	HEADER_5 HEADER_5X1
45	1	P19	POWER12 POWER12
46	3	PA1,PA2,PA3	BUS62 BUS62
47	3	PB1,PB2,PB3	BUS36 BUS36
48	4	Q1,Q2,Q3,Q4	2N2907A SOT23
49	2	Q5,Q6	2N3904 SOT23
50	1	Q7	2N3906 SOT23
51	31	R1,R2,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29,R30,R31	33 0805
52	11	R32,R33,R34,R35,R36,R37, R38,R39,R40,R41,R42	1K 0805
53	22	R44,R45,R46,R47,R48,R49, R50,R51,R52,R53,R54,R55, R57,R58,R59,R60,R61,R62, R80,R166,R167	4.7K 0805
54	1	R63	536_1% 0805
55	10	R64,R66,R67,R68,R69,R70, R71,R72,R73,R74	22 0805
56	17	R75,R76,R77,R78,	0 0805
58	7	R93,R94,R95,R96,R97,R98, R99	75_1% 0805
59	14	R100,R101,R102,R103,R104, R105,R106,R107,R108,R109, R110,R111,R112,R170	10K 0805
60	4	R113,R114,R115,R116	200 0805
61	5	R117,R118,R119,R120,R121	1.2K 0805
62	4	R122,R123,R124,R125	12 0805
63	4	R126,R127,R128,R129	1.8K 0805
64	4	R130,R131,R132,R133	8.2 0805
65	1	R134	3.3K 0805
66	7	R135,R136,R137,R138,R139, R140,R175	2.2K 0805
67	4	R141,R142,R143,R144	300 0805
68	1	R145	10M 0805
69	3	R146,R147,R148	100 0805
70	4	R149,R150,R151,R152	82 0805
71	6	R153,R154,R155,R163,R164, R165	150 0805

72	2	R156,R157	5.6K 0805
73	3	R158,R159,R174	220 0805
74	2	R160,R173	330 0805
75	2	R161,R162	8.2K 0805
76	1	R168	200
77	1	R169	82
78	1	R171	0
79	64	RP1A,RP1B,RP1C,RP1D,RP2A, RP2B,RP2C,RP2D,RP3A,RP3B, RP3C,RP3D,RP4A,RP4B,RP4C, RP4D,RP5A,RP5B,RP5C,RP5D, RP6A,RP6B,RP6C,RP6D,RP7A, RP7B,RP7C,RP7D,RP29A, RP29B,RP29C,RP29D,RP30A, RP30B,RP30C,RP30D,RP31A, RP31B,RP31C,RP31D,RP32A, RP32B,RP32C,RP32D,RP33A, RP33B,RP33C,RP33D,RP34A, RP34B,RP34C,RP34D,RP35A, RP35B,RP35C,RP35D,RP36A, RP36B,RP36C,RP36D,RP37A, RP37B,RP37C,RP37D	CRA4 22
80	16	RP8A,RP8B,RP8C,RP8D,RP9A, RP9B,RP9C,RP9D,RP10A, RP10B,RP10C,RP10D,RP11A, RP11B,RP11C,RP11D	CRA4 2.2K
81	32	RP12A,RP12B,RP12C,RP12D, RP13A,RP13B,RP13C,RP13D, RP14A,RP14B,RP14C,RP14D, RP15A,RP15B,RP15C,RP15D, RP16A,RP16B,RP16C,RP16D, RP17A,RP17B,RP17C,RP17D, RP18A,RP18B,RP18C,RP18D, RP21A,RP21B,RP21C,RP21D	CRA4 8.2K
82	8	RP19A,RP19B,RP19C,RP19D, RP20A,RP20B,RP20C,RP20D	CRA4 5.6K
83	42	RP22A,RP22B,RP22C,RP22D, RP23A,RP23B,RP23C,RP23D, RP26A,RP26B,RP26C,RP26D, RP27A,RP27B,RP27C,RP27D, RP38A,RP38B,RP38C,RP38D, RP39A,RP39B,RP39C,RP39D, RP40A,RP40B,RP40C,RP40D, RP41A,RP41B,RP41C,RP41D, RP42,RP43,RP43C,RP43D, RP44A,RP44B,RP44C,RP44D, RP45,RP46	CRA4 4.7K
84	8	RP24A,RP24B,RP24C,RP24D, RP25A,RP25B,RP25C,RP25D	CRA4 330
85	4	RP28A,RP28B,RP28C,RP28D	CRA4 150
86	2	SW1,SW2	SW_PUSHBUTTON SWCI
87	1	U1	SIP1 BGA388
88	6	U2,U3,U4,U5,U6,U7	74F245 SO20
89	4	U8,U9,U10,U11	SIMM-36BIT SIMM72
90	1	U12	STV0119 SO28
91	1	U13	LF33 DPAK
92	1	U14	MINIDIN4 MINIDIN4
93	4	U15,U16,U17,U18	74F153 SO16
94	1	U19	74F138 SO16

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   95       1    U20                         PC87306VUL PQFP160
   96       2    U21A,U21D                   74F32 SO14
   97       4    U22,U23,U24,U25             74F74V SO14
   98       1    U26                         M27C2001 DIP32
   99       1    U27                         UM8667 SSOP48
  100       4    U28A,U28B,U28C,U28D         74F00 SO14
  101       4    U29A,U29B,U29C,U29D         74LS14 SO14
  102       1    U30                         74F32V SO14
  103       1    U31                         74LS14V SO14
  104       1    U32                         LT1085CT TO220
  105       1    U33                         74F125
  106       1    U34                         74LS14
  108       1    Y2                          32KHz KF38
DO NOT INSTALL
--------------
Y1
R3,R56,R65,R79,R81,R82,R83,R84,R85,R86,R87,R88,R89,R90,R91,R92
C86,C87
STR3CMS
-------
Assemble all in [1-2] position
WIRING MODIFICATIONS
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4.3.3 BOM when using STPC Consumer

EVMINI1.2 Consumer Revised: May 8, 1998
Revision: 1.2

Bill Of Materials May 8, 1998 3:18:11

Item	Quantity	Reference	Part
1	1	B1	3.0V COIN
2	10	C1,C144,C145,C146,C147, C148,C149,C150,C151,C152	10nF 0805
3	69	C2,C3,C4,C5,C6,C7,C8,C9, C10,C11,C12,C13,C14,C15, C16,C17,C18,C19,C20,C21, C22,C23,C24,C25,C26,C27, C28,C29,C30,C31,C32,C33, C34,C35,C36,C37,C38,C39, C40,C41,C42,C43,C44,C45, C46,C47,C48,C49,C50,C51, C52,C53,C54,C140,C153, C154,C155,C156,C157,C158, C159,C160,C161,C162,C163, C164,C165,C173,C174	.1uF 0805
4	9	C55,C56,C61,C62,C63,C64, C65,C66,C67	1uF A
5	10	C57,C58,C59,C60,C166, C167,C168,C169,C170,C171	33uF C
6	19	C68,C69,C70,C71,C72,C73, C74,C75,C76,C77,C78,C79, C80,C81,C82,C83,C84,C85, C143	22uF B
7	4	C86,C87,C88,C89	15pF 0805
8	4	C90,C91,C92,C93	220pF 0805
9	4	C94,C95,C96,C97	330pF 0805
10	14	C98,C99,C100,C101,C102, C103,C104,C105,C131,C132, C133,C134,C135,C136	390pF 0805
11	4	C106,C107,C108,C109	3.3nF 0805
12	11	C110,C111,C112,C113,C114, C115,C116,C117,C118,C119, C120	47pF 0805
13	2	C121,C122	680pF 0805
14	8	C123,C124,C125,C126,C127, C128,C129,C130	470pF 0805
15	3	C137,C138,C139	10uF B
16	2	C141,C142	22uF_16V D
17	1	C172	220uF B
18	1	D1	LM385BZ TO92
19	12	D2,D3,D4,D5,D6,D7,D8,D9, D10,D11,D12,D13	1N4148 SOT23
20	4	D14,D15,D16,D17	BAR43 SOT23
21	4	DL1,DL2,DL3,DL4	LED SOT23 *
22	2	FB1,FB2	FBEAD FERRITE
23	1	HP1	SPEAKER
24	24	J1,J3,J4,J5,J6,J7,J8,J18, J19,J20,J21,J23,J24,J25, J26,J27,J28,J29,J30,J31, J32,J33,J98,J100	JUMPER_2X1 HEADER_2X1
25	17	J34,J35,J36,J37,J38,J39, J40,J41,J42,J43,J44,J45, J46,J47,J48,J49,J50	STR3CMS STR3CMS

26	2	J72,J73	TESTPIN HEADER_1X1
27	3	J92,J93,J99	HEADER_3 HEADER_3X1
28	6	L1,L2,L3,L4,L5,L6	BEAD 1206
29	4	L7,L8,L9,L10	2.7uH 1206
30	1	L11	BEAD
31	1	OS1	OSCP OSCP
32	1	OS2	27MHz
33	1	P1	DBS15F DBS15F
34	2	P2,P3	MINIDIN MINIDIN
35	2	P4,P5	HEADER_13X2 HEADER_13X2
36	1	P6	CINCH_F CINCH_F
37	1	P7	PERITEL SCART
38	3	P8,P9,P10	PCI32 PCI32
39	1	P11	CONNECTOR_DB9 DB9MC
40	1	P12	HEADER_5X2 HEADER_5X2
41	2	P13,P14	HEADER_20X2 HEADER_20X2
42	1	P15	HEADER_17X2 HEADER_17X2
43	1	P17	ATX ATX
44	1	P18	HEADER_5 HEADER_5X1
45	1	P19	POWER12 POWER12
46	3	PA1,PA2,PA3	BUS62 BUS62
47	3	PB1,PB2,PB3	BUS36 BUS36
48	4	Q1,Q2,Q3,Q4	2N2907A SOT23
49	2	Q5,Q6	2N3904 SOT23
50	1	Q7	2N3906 SOT23
51	31	R1,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29,R30,R31	33 0805
52	11	R32,R33,R34,R35,R36,R37, R38,R39,R40,R41,R42	1K 0805
53	22	R44,R45,R51,R52,R53,R55, R56,R57,R58,R59,R60,R61, R62,R80,R166,R167	4.7K 0805
54	1	R63	536_1% 0805
55	10	R64,R66,R67,R68,R69,R70, R71,R72,R73	22 0805
56	17	R65,R79,R81,R82,R83,R84, R85,R86,R87,R88,R89,R90, R91	0 0805
57	1	R92	1M 0805
58	7	R93,R94,R95,R96,R97,R98, R99	75_1% 0805
59	14	R100,R101,R102,R103,R104, R105,R106,R107,R108,R109, R110,R111,R112,R170	10K 0805
60	4	R113,R114,R115,R116	200 0805
61	5	R117,R118,R119,R120,R121	1.2K 0805
62	4	R122,R123,R124,R125	12 0805
63	4	R126,R127,R128,R129	1.8K 0805
64	4	R130,R131,R132,R133	8.2 0805
65	1	R134	3.3K 0805
66	7	R135,R136,R137,R138,R139, R140,R175	2.2K 0805
67	4	R141,R142,R143,R144	300 0805
68	1	R145	10M 0805
69	3	R146,R147,R148	100 0805
70	4	R149,R150,R151,R152	82 0805

71	6	R153,R154,R155,R163,R164, R165	150 0805
72	2	R156,R157	5.6K 0805
73	3	R158,R159,R174	220 0805
74	2	R160,R173	330 0805
75	2	R161,R162	8.2K 0805
76	1	R168	200
77	1	R169	82
79	64	RP1A,RP1B,RP1C,RP1D,RP2A, RP2B,RP2C,RP2D,RP3A,RP3B, RP3C,RP3D,RP4A,RP4B,RP4C, RP4D,RP5A,RP5B,RP5C,RP5D, RP6A,RP6B,RP6C,RP6D,RP7A, RP7B,RP7C,RP7D,RP29A, RP29B,RP29C,RP29D,RP30A, RP30B,RP30C,RP30D,RP31A, RP31B,RP31C,RP31D,RP32A, RP32B,RP32C,RP32D,RP33A, RP33B,RP33C,RP33D,RP34A, RP34B,RP34C,RP34D,RP35A, RP35B,RP35C,RP35D,RP36A, RP36B,RP36C,RP36D,RP37A, RP37B,RP37C,RP37D	CRA4 22
80	16	RP8A,RP8B,RP8C,RP8D,RP9A, RP9B,RP9C,RP9D,RP10A, RP10B,RP10C,RP10D,RP11A, RP11B,RP11C,RP11D	CRA4 2.2K
81	32	RP12A,RP12B,RP12C,RP12D, RP13A,RP13B,RP13C,RP13D, RP14A,RP14B,RP14C,RP14D, RP15A,RP15B,RP15C,RP15D, RP16A,RP16B,RP16C,RP16D, RP17A,RP17B,RP17C,RP17D, RP18A,RP18B,RP18C,RP18D, RP21A,RP21B,RP21C,RP21D	CRA4 8.2K
82	8	RP19A,RP19B,RP19C,RP19D, RP20A,RP20B,RP20C,RP20D	CRA4 5.6K
83	42	RP22A,RP22B,RP22C,RP22D, RP23A,RP23B,RP23C,RP23D, RP26A,RP26B,RP26C,RP26D, RP27A,RP27B,RP27C,RP27D, RP38A,RP38B,RP38C,RP38D, RP39A,RP39B,RP39C,RP39D, RP40A,RP40B,RP40C,RP40D, RP41A,RP41B,RP41C,RP41D, RP42,RP43,RP43C,RP43D, RP44A,RP44B,RP44C,RP44D, RP45,RP46	CRA4 4.7K
84	8	RP24A,RP24B,RP24C,RP24D, RP25A,RP25B,RP25C,RP25D	CRA4 330
85	4	RP28A,RP28B,RP28C,RP28D	CRA4 150
86	2	SW1,SW2	SW_PUSHBUTTON SWCI
87	1	U1	SIP1 BGA388
88	6	U2,U3,U4,U5,U6,U7	74F245 SO20
89	4	U8,U9,U10,U11	SIMM-36BIT SIMM72
91	1	U13	LF33 DPAK
92	1	U14	MINIDIN4 MINIDIN4
93	4	U15,U16,U17,U18	74F153 SO16
94	1	U19	74F138 SO16

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   95       1    U20                         PC87306VUL PQFP160
   96       2    U21A,U21D                   74F32 SO14
   97       4    U22,U23,U24,U25             74F74V SO14
   98       1    U26                         M27C2001 DIP32
   99       1    U27                         UM8667 SSOP48
  100       4    U28A,U28B,U28C,U28D         74F00 SO14
  101       4    U29A,U29B,U29C,U29D         74LS14 SO14
  102       1    U30                         74F32V SO14
  103       1    U31                         74LS14V SO14
  104       1    U32                         LT1085CT TO220
  105       1    U33                         74F125
  106       1    U34                         74LS14
  107       1    Y1                          14.3MHz HC49U
  108       1    Y2                          32KHz KF38
MAY NOT BE INSTALLED
--------------------
C13,C22,C54,C71
L6
OS1
U15
DO NOT INSTALL
--------------
R2,R46,R47,R48,R49,R50,R74,R54,R75,R76,R77,R78,R171
U12
STR3CMS
-------
Assemble all in [2-3] position exect J36 and J37 ([1-2])
WIRING MODIFICATIONS
--------------------
```

4.4 How to design for both PC Client and PC Consumer

This chapter describes how to make a board design for both ST PC Client and ST PC Consumer (A.N. H97001 - Release 1.2 - 24/12/97).

4.4.1 Differences between STPC Client and STPC Consumer

4.4.1.1 Functionnal differences.

The ST PC Client is historically the first device of ST PC Family.
The ST PC Consumer's main external difference with its predecessor is the analog TV output instead of a digital one.

TABLE 37. STPC Client and STPC Consumer functionnal differences

ST PC Client	ST PC Consumer
Needs an oscillator for internal clocks generation	Needs a quartz for internal clocks generation
Digital TV output	Analog TV output
10 reserved pins	Only 1 reserved pin

4.4.1.2 Pinout differences.

For technical reasons, 49 signals were changed or moved from ST PC Client to ST PC Consumer on which 10 are just renamed.

TABLE 38. STPC Client and STPC Consumer pinout differences

ST PC	Client	ST PC	Consumer	
Pin	**Signal Name**	**Pin**	**Signal Name**	**Comment**
AF10	TV_YUV[0]			Removed
AC10	TV_YUV[1]			Removed
AE11	TV_YUV[2]			Removed
AD10	TV_YUV[3]			Removed
AF11	TV_YUV[4]			Removed
AE12	TV_YUV[5]			Removed
AF12	TV_YUV[6]			Removed
AD11	TV_YUV[7]			Removed
AD9	VTV_BT#	AD9	ODD_EVEN	Renamed
AE10	VTV_HSYNC	AE10	VCS	Renamed
B4	ST[0]			Removed
D5	ST[1]			Removed
A4	ST[2]			Removed

TABLE 38. STPC Client and STPC Consumer pinout differences

ST PC	Client	ST PC	Consumer	
C5	ST[3]			Removed
B3	ST[4]			Removed
C4	ST[5]	C5	SPKRD	Renamed & Moved
A3	ST[6]			Removed
C7	CLKDEL[0]			Removed
B5	CLKDEL[1]			Removed
A5	CLKDEL[2]			Removed
AF5	DCLK_DIR			Removed
D24	PCI_INT[0]	A5	PCI_INT[0]	Moved
C26	PCI_INT[1]	C6	PCI_INT[1]	Moved
A25	PCI_INT[2]	B4	PCI_INT[2]	Moved
B24	PCI_INT[3]	D5	PCI_INT[3]	Moved
AD14	VIDEO_CLK	AC12	VCLK	Renamed & Moved
AE13	VIDEO_D[0]	AE13	VIN[0]	Renamed
AC12	VIDEO_D[1]	AD14	VIN[1]	Renamed & Moved
AD12	VIDEO_D[2]	AD12	VIN[2]	Renamed
AE14	VIDEO_D[3]	AE14	VIN[3]	Renamed
AC14	VIDEO_D[4]	AC14	VIN[4]	Renamed
AF14	VIDEO_D[5]	AF14	VIN[5]	Renamed
AD13	VIDEO_D[6]	AD13	VIN[6]	Renamed
AE15	VIDEO_D[7]	AE15	VIN[7]	Renamed
AF15	XTALI	A3	XTALI	Moved
AE16	XTALO	C4	XTALO	Moved
W4	VDD_GCLK_PLL	AD19	VDD_GCLK_PLL	Moved
AB1	VDD_DCLK_PLL	AF13	VDD_DCLK_PLL	Moved
C6	OSC14M	AF8	OSC14M	Moved
AD8	DDC[0]	C7	DDC[0]	Moved
AF8	DDC[1]	B5	DDC[1]	Moved
AD5	DCLK	AF9	DCLK	Moved
AC5	GCLK2X	AF15	GCLK2X	Moved
AF9	HSYNC	AC5	HSYNC	Moved
AE9	VSYNC	AD5	VSYNC	Moved
AC9	COMP	AF5	COMP	Moved
AF13	VDD	AB1	VDD	Moved
AD19	VDD	W4	VDD	Moved
AD7	VREF	AD7	VREF_DAC	Renamed
		AE16	VSS	New
		AF10	RED_TV	New
		AC10	GREEN_TV	New

TABLE 38. STPC Client and STPC Consumer pinout differences

ST PC	Client	ST PC	Consumer	
		AF11	BLUE_TV	New
		AD11	CVBS	New
		AD8	IREF1_TV	New
		AE11	IREF2_TV	New
		AE9	VREF1_TV	New
		AD10	VREF2_TV	New
		AF12	VDDA_TV	New
		AE12	VSSA_TV	New
		A4	RTCAS#	New
		AC9	ZWS#	New
		B3	SCAN_ENABLE	New

4.4.2 Signal multiplexing

4.4.2.1 Constraints.

There are several ways to design a board which accept both components.

TABLE 39. Possible choices when multiplexing signals

Solution	Advantages	Drawbacks
2 footprints	simple schematics simple BOM flexible (if socket)	increase board size + increase routing complexity + longer nets + cost
1 footprint Multiplexors	space on board simple BOM flexible (if socket)	complex schematics increase board size increase routing complexity longer nets net delay and loading are modified cost
1 footprint 0 ohms resistors Different BOMs	space on board + system speed cost	complex schematics + not flexible two BOMs

For our evaluation board, for example, we wanted a small board with low price and the best performance, we chose to use the 0 ohm resistor solution.

4.4.2.2 Solution

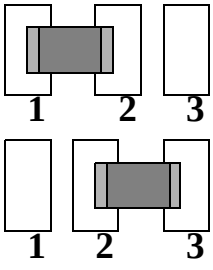
TABLE 40. Solution using null resistors as multiplexors and multiple BOMs.

Pin	Signal [Client] Signal [Consumer]	Connecting component	Signal of the Board
D26,C26,A25,B24	PCI_INT[0:3] Unconnected	0 ohm -	PCI_INT[0:3] -
C7, B5	CLKDEL[0:1] DDC[0:1]	4K7 pullup 0 ohm	3.3V DDC[0:1]
A5	CLKDEL[2] PCI_INT[0]	4K7 pullup 0 ohm	3.3V PCI_INT[0]
B4,D5	ST[0:1] PCI_INT[2:3]	4K7 pullup 0 ohm	3.3V PCI_INT[2:3]
A4	ST[2] RTCAS#	4K7 pullup 0 ohm	3.3V RTCAS#
C5	ST[3] SPKRD	4K7 pullup 0 ohm	3.3V SPKRD
B3	ST[4] SCAN_ENABLE	- 4K7 pulldown	- GND
C4	ST[5] XTALO	0 ohm 0 ohm	SPKRD XTALO
A3	ST[6] XTALI	- 0 ohm	- XTALI
AD14	VIDEO_CLK VIN[1]	0 ohm 0 ohm	VIDEO_CLK VIN[1]
AC12	VIDEO_D[1] VCLK	0 ohm 0 ohm	VIDEO_D[1] VCLK
AD8	DDC[0] IREF1_TV	0 ohm 0 ohm	DDC[0] IREF1_TV
AF8	DDC[1] OSC14M	0 ohm 0 ohm	DDC[1] 3.3V
AF15	XTALI GCLK2X	0 ohm -	XTALI -
AE16	XTALO VSS	0 ohm 0 ohm	XTALO GND
C6	OSC14M PCI_INT[1]	0 ohm 0 ohm	OSC14M PCI_INT[1]
W4	VDD_GCLK_PLL VDD	Wire Wire	3.3V 3.3V
AB1	VDD_DCLK_PLL VDD	Wire Wire	3.3V 3.3V
AD19	VDD VDD_GCLK_PLL	Wire Wire	3.3V 3.3V
AF13	VDD VDD_DCLK_PLL	Wire Wire	3.3V 3.3V
AD5	DCLK VSYNC	0 ohm 0 ohm	DCLK VSYNC

TABLE 40. Solution using null resistors as multiplexors and multiple BOMs.

Pin	Signal [Client] Signal [Consumer]	Connecting component	Signal of the Board
AC5	GCLK2X HSYNC	- 0 ohm	- HSYNC
AF9	HSYNC DCLK	0 ohm 0 ohm	HSYNC DCLK
AF5	DCLK_DIR COMP	4K7 pulldown 0 ohm	GND COMP
AC9	COMP ZWS#	0 ohm 0 ohm	COMP ZWS#
AE9	VSYNC VREF1_TV	0 ohm 0 ohm	VSYNC VREF1_TV
AF10	TV_YUV[0] RED_TV	0 ohm 0 ohm	TV_YUV[0] RED_TV
AC10	TV_YUV[1] GREEN_TV	0 ohm 0 ohm	TV_YUV[1] GREEN_TV
AE11	TV_YUV[2] IREF2_TV	0 ohm 0 ohm	TV_YUV[2] IREF2_TV
AD10	TV_YUV[3] VREF2_TV	0 ohm 0 ohm	TV_YUV[3] VREF2_TV
AF11	TV_YUV[4] BLUE_TV	0 ohm 0 ohm	TV_YUV[4] BLUE_TV
AE12	TV_YUV[5] VSSA_TV	0 ohm 0 ohm	TV_YUV[5] AGND
AF12	TV_YUV[6] VDDA_TV	0 ohm 0 ohm	TV_YUV[6] Analog 3.3V
AD11	TV_YUV[7] CVBS	0 ohm 0 ohm	TV_YUV[7] CVBS
AE10	VTV_HSYNC VCS	0 ohm 0 ohm	VTV_HSYNC VCS
AD9	VTV_BT# ODD_EVEN	0 ohm 0 ohm	VTV_BT# ODD_EVEN

The configuration 0 ohm twice in the same ‘connecting component’ box is done using a 0 ohm multiplexor. This is achieved using a 3-pad SMD footprint where you put a 0 ohm resistor in the one of the two possible locations. Using a 0805 SMD resistor, this assume a very small multiplexor with good electrical characteristics.



In addition to this table, we must take into account the external STV0119 used with the ST PC Client. If it is always on the board, TV_YUV[0:7], VTV_HSYNC and VTV_BT# must be connected through the 0 ohm resistors in the table. If it is not installed with the ST PC Consumer (recommended choice) the number of 0 ohm resistors can be reduced.

For analog signals with electrical constraints like voltage references and current references, it is possible to duplicate the discrete components connected and to place one of each set near the corresponding component.
For example, capacitors and resistors on VREFxx and IREFxx lines can be duplicated. One set is assembled only when the STV0119 is on board (ST PC Client), the other set is assembled only when the ST PC Consumer in present.

4.4.3 Example

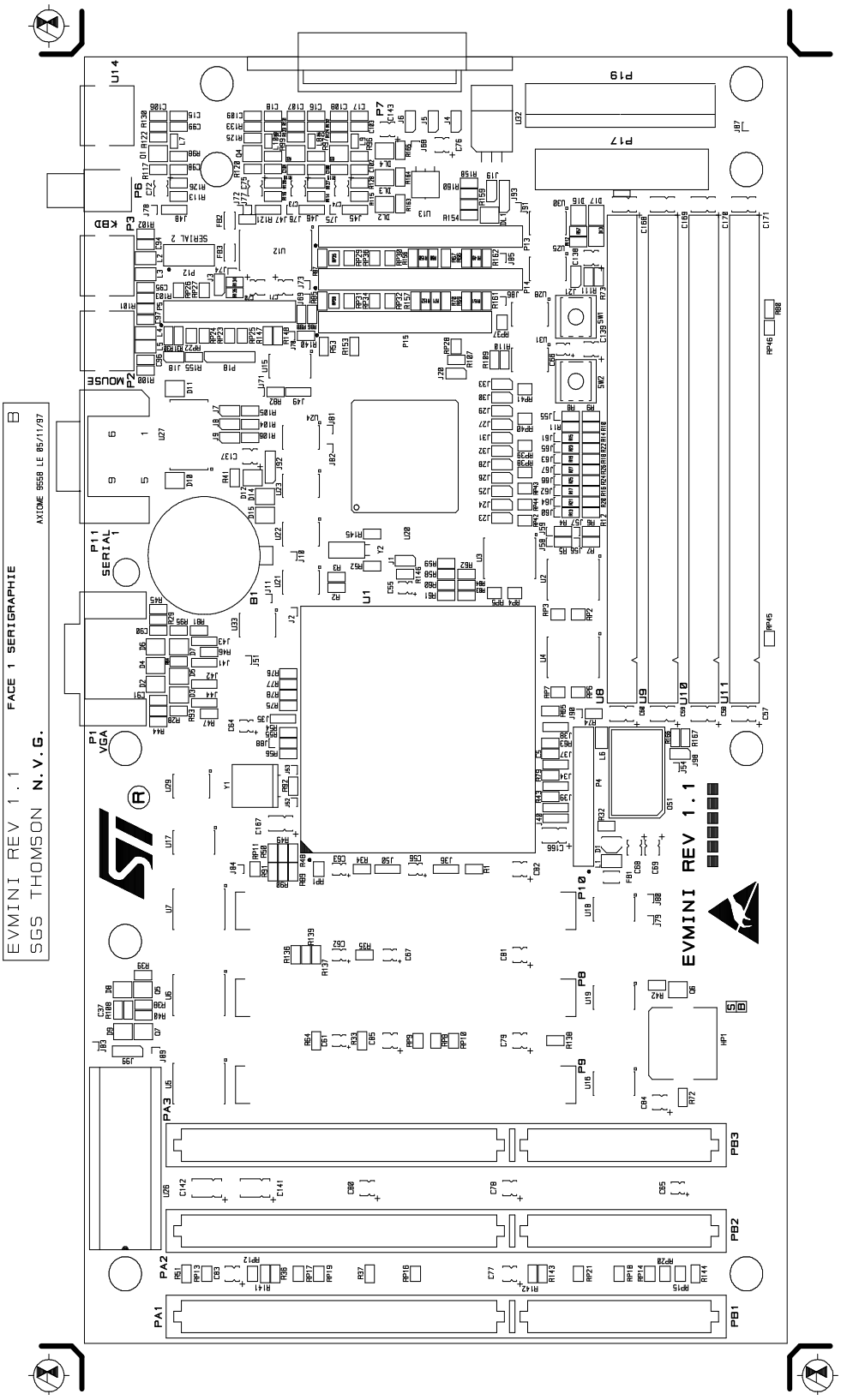
see schematics in this document or download the up to date Reference Design (ST / NVG intranet web page).

4.4.4 Application Note History

Release 1.0: First Release.
Release 1.1: Update due to improved STPC Consumer pinout.
Release 1.2: Update due to external DCLK Video Clock (27MHz).

4.5 PCB

4.5.1 Silkscreen



4.6 Electrical Specifications

The Power Supply used to power this board must have the characteristics detailed in the following table.

TABLE 41. Power Supply Characteristics

Voltage	Precision
+5V	+/- 250mV
+12V	+/- 600mV
-5V	+/-500mV
-12V	+/- 1.2V
+3.3V	+/- 300mV

5. Motherboard Software Specifications.

5.1 System Address Map:

This section describes the mapping of the CPU memory and IO address spaces. Also covered in this section are the PCI configuration space mapping

5.1.1 Memory Address Map.

TABLE 42. Memory Address Map

Address Range (Dec)	Address Range (Hex)	Size	Description
1024K-16984K	100000-1000000	15960K	Extended Memory
896K-1024K	0E0000-0FFFFF	128K	System Bios
768K-800K	0C0000-0C7FFF	32K	Graphic Bios
736K-768K	0B8000-0BFFFF	32K	Monochrome Text Memory
704K-736K	0B0000-0B7FFF	32K	Color Text Memory
640K-704K	0A0000-0AFFFF	64K	“Graphic” Memory
0K-640K	0-9FFFF	640K	Conventional Memory

5.1.2 IO Address MAP

The system chip-set implements a number of registers in IO address space. These register occupy the following map in the IO space.

TABLE 43. IO Address Map

Address Range (Hex)	Size (Hex)	Description
0000-000F	16 Bytes	DMA Controller 1 (8237)
0020-0021	2 Bytes	Interrupt Controller 1 (8259)
0022-0023	2 Bytes	ST486 Specific Registers
0040-0043	4 Bytes	Timer Controller (8254)
0060	1 Bytes	Keyboard Controller Data Byte
0061	1 Byte	NMI, Speaker Control
0064	1 Byte	Kbd Ctlr, CMD,STAT Byte
0070, bit 7	1 bit	Enable
0070, bit6:0	7 bits	Real Time Clock Address
0078	1 Byte	General Purpose I/O
0080-008F	16 Bytes	DMA Page Registers
00A0-00A1	2 Bytes	Interrupt Controller 2 (8259)
00C0-00DE	31 Bytes	DMA Controller 1 (8237)
00F0	1 Byte	Reset Numeric Error
0102	1 Byte	VGA Setup Register
0170-0177	8 Bytes	Secondary IDE Channel
01F0-01F7	8 Bytes	Primary IDE Channel
0278-027B	4 Bytes	Parallel Port 2 (Bidir)
02F8-02FF	8 Bytes	Serial Port 2
0378-037F	8 Bytes	Parallel Port 1
03B4, 03B5, 03BA	3 bytes	VGA Registers
03D4, 03D5, 03DA	3 Bytes	VGA Registers
03C0-03CF	16 Bytes	VGA Registers
03F0-03F5	6 Bytes	Floppy Controller Registers
03F6	1 Byte	IDE Command Port
03F7 (Write)	1 Byte	Floppy Command Port
03F7, bit 7	1 bit	Floppy Disk Change
03F7, bits 6:0	7 bits	IDE Status Port
03F8-03FF	8 Bytes	Serial Port 2
0CF8	1 Byte	PCI Configuration Address Register
0CFC-0CFF	8 Bytes	PCI Configuration Data Registers
046E8	1 Byte	VGA Add-in mode enable Register
C000-C0FF	256 Bytes	PCI Configuration Registers

5.2 Interrupts and DMA Channels

TABLE 44. IRQ Channels

IRQ	System Resource
NMI	Parity Error
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer Full
2	Reserved, Cascade Interrupt from Interrupt Controller 2
3	Serial Port 2
4	Serial Port 1
5	Parallel Port 2 (P10)
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	User available (video)
10	User available
11	User available
12	PS/2 Mouse Port
13	Reserved, Math coprocessor
14	IDE
15	User available / IDE

TABLE 45. DMA Channels

DMA	Data Width	System Resource
0	8 bits	User available
1	8 bits	User available
2	8 bits	Floppy
3	8 bits	Parallel Port
4		Reserved, Cascade Channel
5	16 bits	IDE Controller
6	16 bits	User Available
7	16 bits	User Available

6. Document History.

Release0.9: 7/9/98 - First Release